Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.047”**

**.047”**

**ANODE**

**.032”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .032” X .032”**

**Backside Potential: Cathode**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .047” DATE: 9/21/21**

**MFG: ON SEMI THICKNESS .016” P/N: MURC110**

**DG 10.1.2**

#### Rev B, 7/19/02